Report for midterm project:

team number 42

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&

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In our project we design the BBQM in some modules

We have 8 modules in our project

**we have Counter module**

**In that module we have up down counter that count up and down and it has its input and output**

INPUT

**1.Up\_Down buttons** which identify we will count up or down .

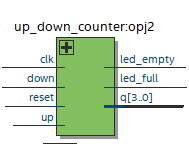
2.**CLK** which is come from the flip flop and have CLK\_divider .

3. **RESET** and that is a reset case in which we back to our initial case(the queue have zero and no tellers) .

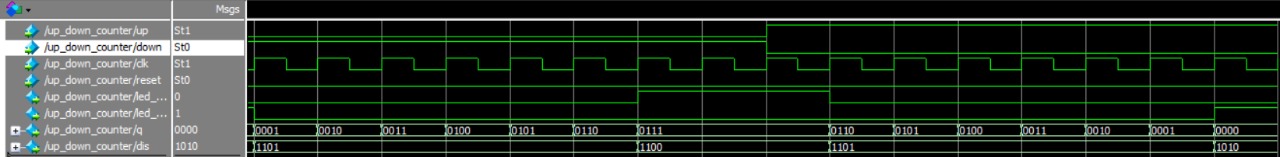
OUTPUT

1. **Count** [3:0] which has wire to decoder\_7 seg to display the output on 7\_segment

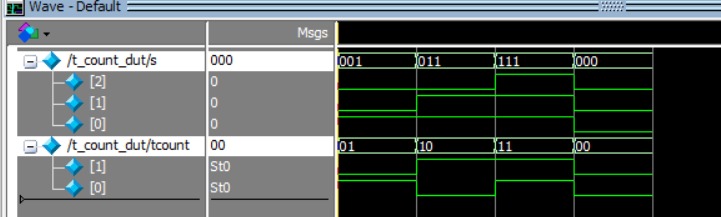
2. **Alarm** and it is a led when the queue is full or empty it is on otherwise it is off



This is the test bench on model Sim For up/down Counter



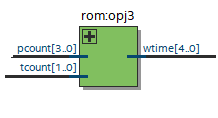
Test bench for tcount



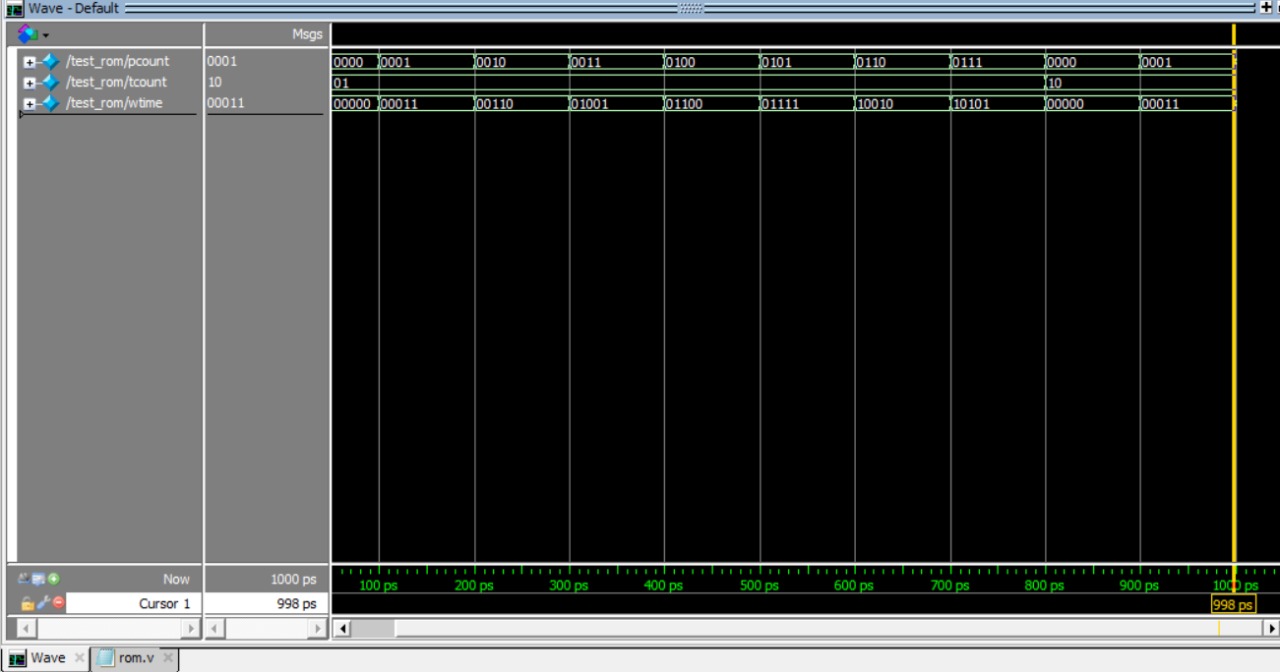
**The rom module**

ROM is declared as a one-dimension array of integers holding the Wtime values. The index into this array could be constructed by concatenating Tcount and Pcount.

**Wtime**=3\*(Pcount+Tcount-1)/Tcount



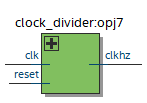
This is our testbench for rom when t (from 1to3) and pcount (from 0 to 7) .

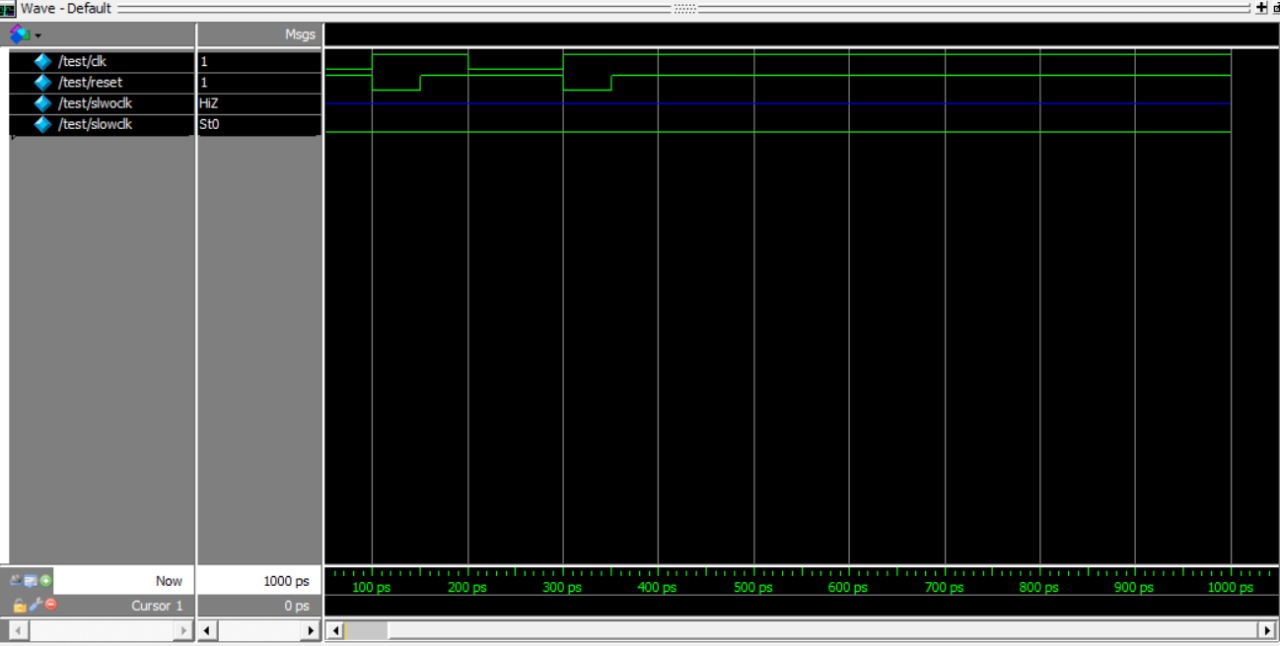


**CLK\_Divider** **Module**

It takes input from the clk which exact on FPGA and from reset switch if it up then the system back to initial state

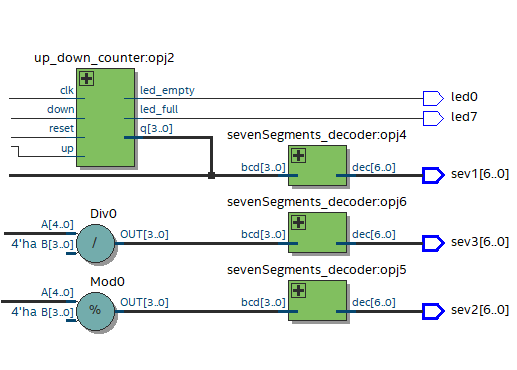
We use that module to create lower frequency. The clk signal has input from an input clk source. The divider circuit count input clk cyclesand drive output clk low and then high for some number of input clk cycles

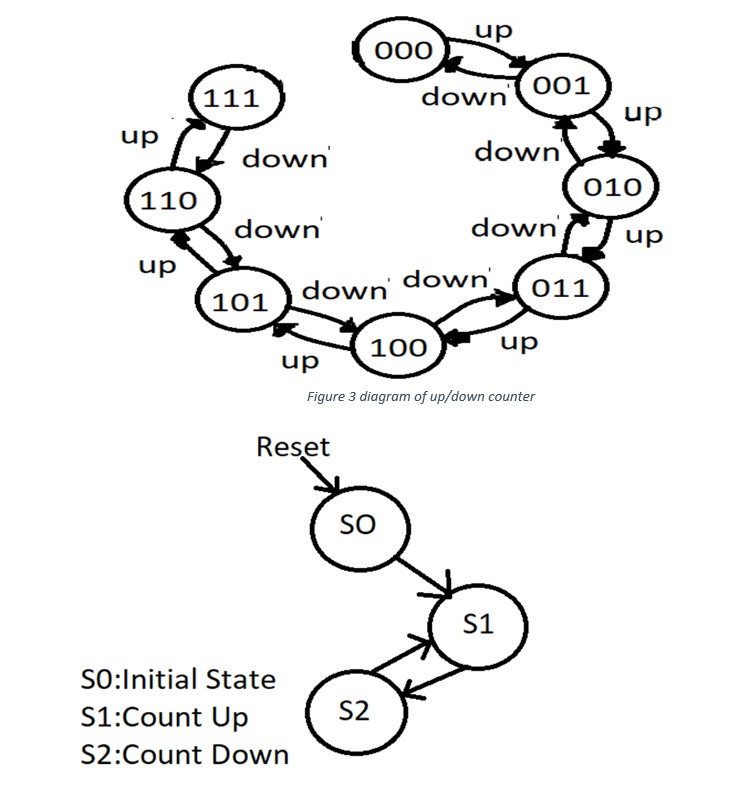




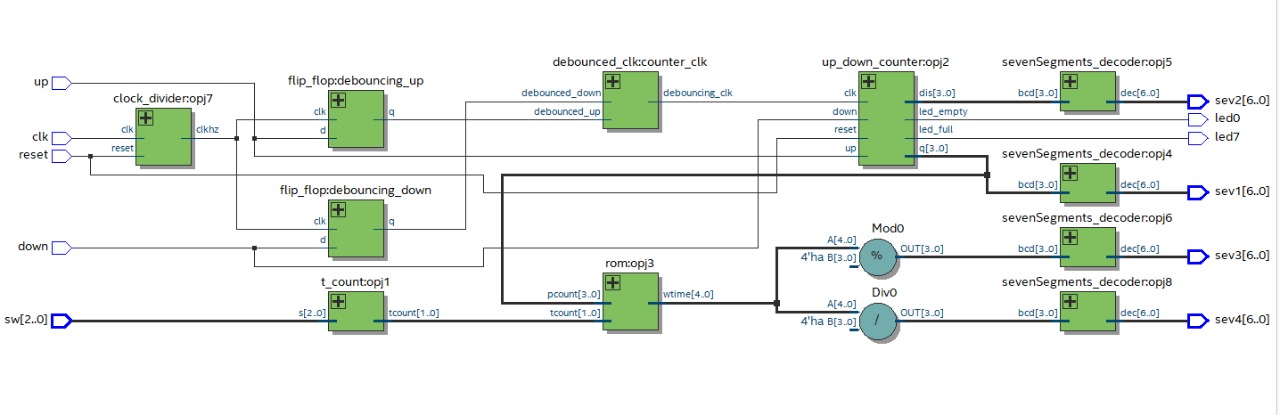
**decoder\_7seg module**

take the input from the up down counter and ROM and then to decoder then to display it on 7 segment on FPGA





**All the project on RTL\_Viewer on quartus**



**TABLE OF TOP MOUDLE**

|  |  |  |
| --- | --- | --- |
| NAME | INPUT/OUPUT | Description |
| PUSHUP | Input | **Increment One When Client Enters the Queue** |
| PUSHDOWN | Input | **Decrement One When Client Enters the Queue** |
| RESET | Input | **Reset The System** |
| TCOUNT | Input | **Number of Tellers** |
| PCOUNT | Output | **Number Of the Clients** |
| Wtime | Output | |  |  |  |  | | --- | --- | --- | --- | |  | |  | | --- | | **Waiting Time for Clients in Queue** | |  | | |
| FULLflag | Output | **The Queue is Full** |
| EMPTYflag | Output | **The Queue is Empty** |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Reset | Up/ | T2 | T1 | |  | Pcount | |  | Wtime |  |  |  | Eflag | Fflag |
|  | Down |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
|  |  |  |  |  | deci |  | 7seg | decimal | 7seg (2) | 7seg (1) | | | Active | Active |
|  |  |  |  |  | mal |  |  |  |  |  |  |  | high | high |
|  |  |  |  | |  |  |  |  |  |  | | |  |  |
| 1 | X | X | X | | 0 |  | 1000000 | 0 | 1111110 | 1111110 | | | 1 | 0 |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
| 0 | up | 0 | 1 |  | 1 |  | 1111001 | 3 | 1111110 | 1111001 | | | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
| 0 | up | 0 | 1 |  | 2 |  | 0100100 | 6 | 1111110 | 1011111 | | | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
| 0 | up | 0 | 1 |  | 7 |  | 1110000 | 21 | 1101101 | 0110000 | | | 0 | 1 |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
| 0 | down | 1 | 0 |  | 6 |  | 0000010 | 10 | 0110000 | 1111110 | | | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
| 0 | down | 1 | 0 |  | 5 |  | 0010110 | 9 | 1111110 | 1111011 | | | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  | | |  |  |
| 0 | down | 1 | 0 |  | 0 |  | 1000000 | 0 | 1111110 | 1111110 | | | 1 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Testbench top model**

